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STUDY ANALYSIS OF ULTRA LOW POWER SRAM CELL USING NANOSCALE TECHNIQUES

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ABSTRACT

Power consumption has become a critical concern in both high performance and portable applications. Methods for power reduction based on the application of adiabatic techniques to CMOS circuits have recently come under renewed investigation. In thermodynamics, an adiabatic energy transfer through a dissipative medium is one in which losses are made arbitrarily small by causing the transfer to occur sufficiently slowly. In this work adiabatic technique is used for reduction of average power dissipation. Analysis of SRAM cell has been done for 180nm CMOS technology. It shows that average power dissipation is reduced up to 75% using adiabatic technique and also shows the effect on static noise margin.

KEYWORDS: CMOS, SRAM, Adiabatic, VLSI.

1. INTRODUCTION

Technology trends have resulted in static power dissipation (leakage) emerging as a first class design consideration in high-performance processor design. Historically, architectural innovations for improving performance relied on exploiting ever larger numbers of transistors operating at higher frequencies. To keep the resulting switching power dissipation at bay, successive technology generations have relied on reducing the supply voltage. In order to maintain performance, however, a corresponding reduction in the transistor threshold voltage (*Vt*) is required. Since the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) sub-threshold leakage current increases exponentially with a reduced *Vt*, static power dissipation has grown to be a significant fraction of overall chip power dissipation in modern, deep-sub-micron (< 0.18μm) processes. Since leakage power is proportional to the number of transistors, much of the recent work in reducing static power has focused on Static Random Access Memory (SRAM)-based structures, such as the caches, that comprise the vast majority of on-chip transistors. Existing circuit-level leakage reduction techniques are oblivious to program behavior and trade off performance for reduced leakage where possible.

2. MATERIALS AND METHODS

2.1 Static/Dynamic Power

Off-state leakage is *static power*, current that leaks through transistors even when they are turned off. The other is *dynamic power*, which arises from the repeated capacitance charge and discharge on the output of the hundreds of millions of gates in today's chips. Dynamic power is proportional to the square of supply voltage, so reducing the voltage significantly reduces power consumption.
Overall power consumption is the sum of dynamic and static power: $P = ACV^2f + VI$leak

The first term is the dynamic power lost from charging and discharging the processor's capacitive loads: *A* is the fraction of gates actively switching and *C* is the total capacitance load of all gates. The second term models the static power lost due to leakage current, *I*leak. When dynamic power is the dominant source of power

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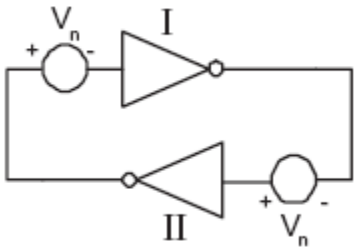
consumption we can approximate above equation with just the first term. Its V^2 factor suggests reducing supply voltage as the most effective way to decrease power consumption. In fact, halving the voltage will reduce the power consumption by a factor of four. Unlike dynamic power, leakage is not activity based, so reducing node switching when there is no work does not help reduce power consumption. Shutting off the inactive part of the system does help, but it results in loss of state.

2.2 Static Noise Margin(SNM)

The stability of SRAM cells determines its soft-error rate and its sensitivity to process tolerances and operating conditions. In many cases, the stability of the cell is a critical factor to obtain a desired yield and to lower the cost of the chip. Many different tests and methods exist that try to capture different aspects of the cell's stability. One of these method is the Static Noise Margin (SNM) Static noises are DC disturbances such as offsets and mismatches due to process variations and changes in operating conditions. The SNM of an SRAM cell is the maximum value of DC disturbances that can be tolerated before the cell's storage value is flipped. Fig. shows the storage elements of the SRAM cell where the static noise sources, *Vn* are included explicitly. The SNM of SRAM cells can be determined graphically by drawing and mirroring the inverter voltage characteristics and finding the maximum possible square between them as shown in Fig. (*Vright* and *Vleft* in Fig. are the input voltages of the bottom and top inverters in Fig. respectively.) The SNM can be thought as the noise voltage necessary at each of the cell storage nodes to shift the curve of the



Back-to-back inverters comprising SRAM cell where static-noise voltage source are included

two cell inverters vertically or horizontally so that they intersect at only one point, where the cell no longer can reliably store a value. The SNM is measured during the read, since the cell is most vulnerable when the pass-transistors are conducting.

SUB-THRESHOLD digital circuit design has emerged as a low energy solution for applications with strict energy constraints. Analysis of sub-threshold designs has focused on logic circuits. SRAMs comprise a significant percentage of the total area for many digital chips as well as the total power. For this reason, SRAM leakage can dominate the total leakage of the chip, and large switched capacitances in the bitlines and wordlines make SRAM accesses costly in terms of energy. Pushing SRAM operation into the sub-threshold region reduces both leakage power and access energy. Also, for system integration, SRAM must become capable of operating at sub-threshold voltages that are compatible with sub-threshold combinational logic. Recent low power memories show a trend of lower voltages with some designs holding state on the edge of the sub-threshold region. This scaling promises to continue, leading to sub-threshold storage modes and even sub-threshold operation for SRAMs operating in tandem with sub-threshold logic.

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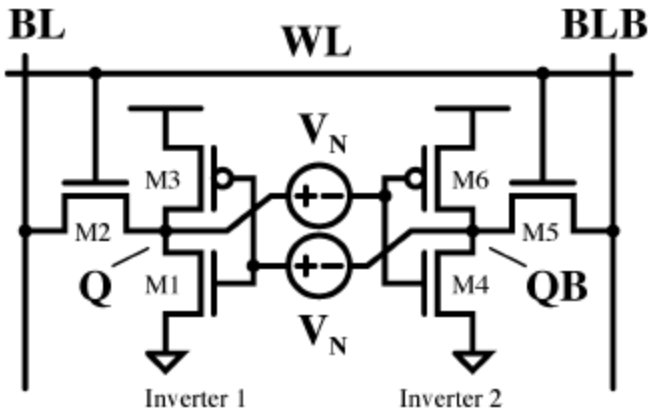

Figure: Schematic for 6T bitcell showing voltage noise sources for finding SNM.

When the bitcell is holding data, its wordline is low so the nMOS access transistors are off. In order to hold its data properly, the back-to-back inverters must maintain bi-stable operating points. The best measure of the ability of these inverters to maintain their state is the bitcell's static noise margin (SNM). The SNM is the maximum amount of voltage noise that can be introduced at the outputs of the two inverters such that the cell retains its data. SNM quantifies the amount of voltage noise required at the internal nodes of a bitcell to flip the cell's contents. Fig. shows a conceptual setup for modeling SNM . Noise sources having value are introduced at each of the internal nodes in the bitcell. As increases, the stability of the cell changes. Fig. shows the most common way of representing the SNM graphically for read access of the cell.

3. RESULTS AND DISCUSSION

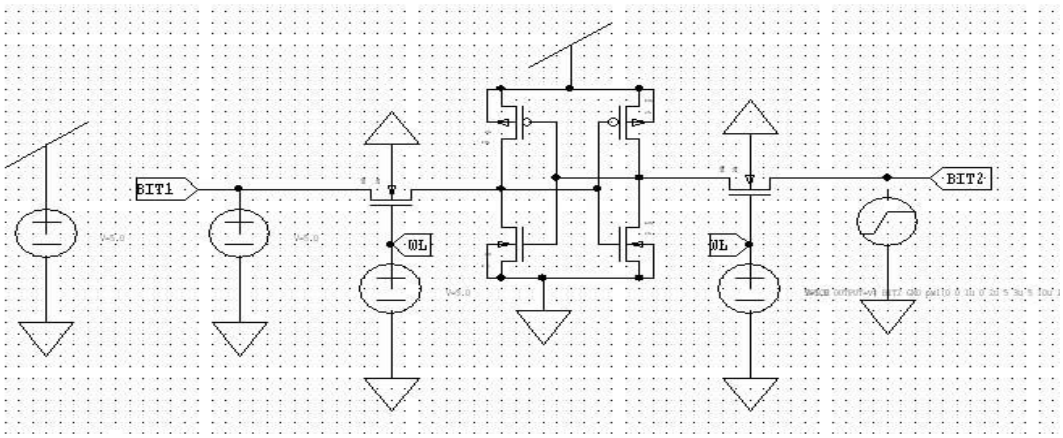

Figure: Schematic of 6T SRAM (L=2u, Vdd=5V)

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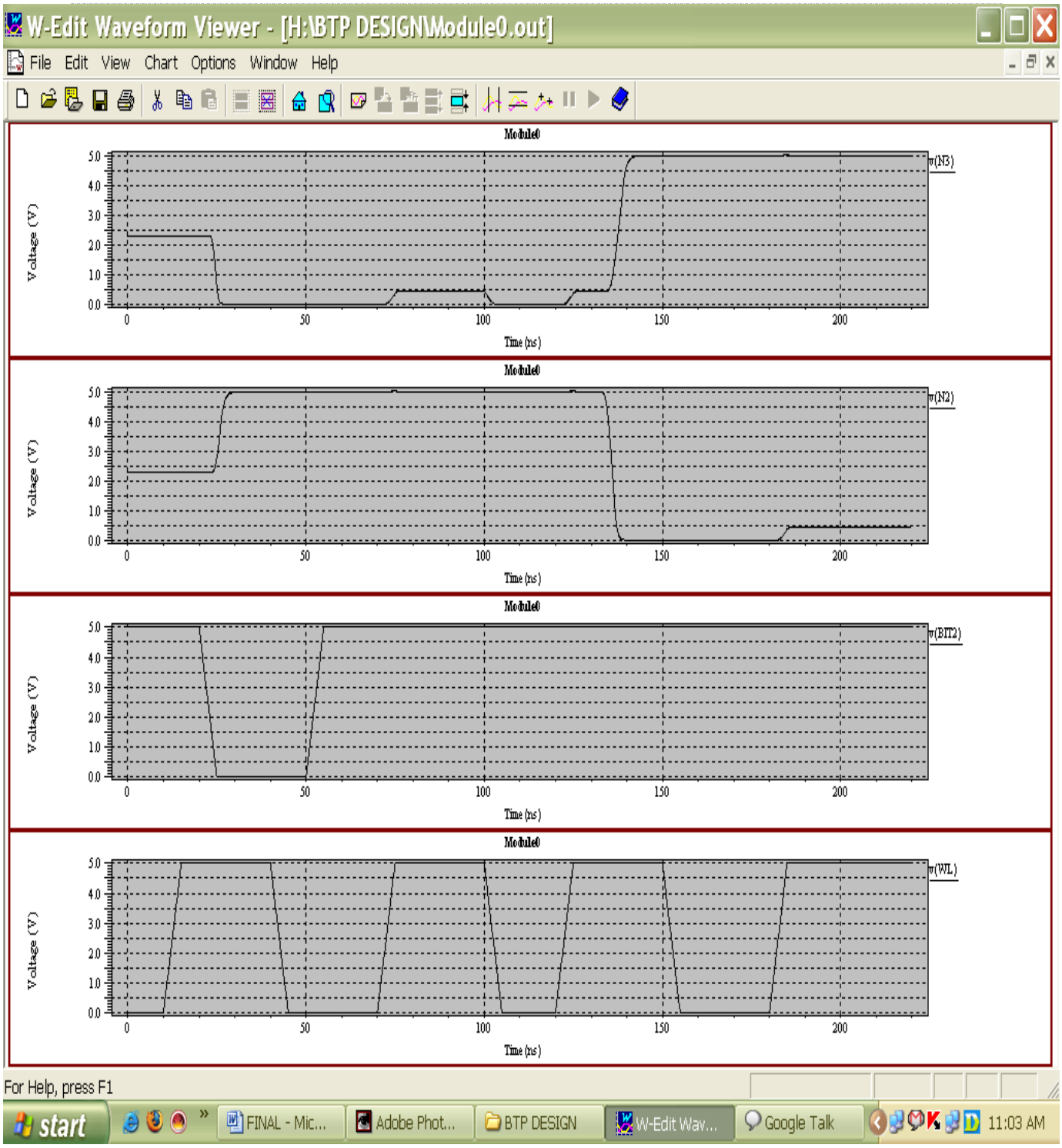

Figure: Voltage pattern for write and read operations on a conventional 6T SRAM cell

4. CONCLUSION

The design of a low power structure for the Static Random Access Memory, involved a detail study of the working of SRAM. We were implementing the design at 90nm technology node, where leakage and static power dissipation play a major limiting role. So we had to look for appropriate methods that would reduce the leakage. After the study of various schemes, we proposed a new SRAM cell based on a Dynamic Voltage Biasing scheme.

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By reduction of cell power supply and raising ground level during standby and changing the well bias voltages we achieved significant reduction in leakage current. For this we first designed the schematic of SRAM cell and the drivers circuits and obtained their correct working by simulating the waveforms. Encouraged by the results, we further investigated the behaviour of memory based on the proposed cell architecture, which also showed marked positive results. We initially planned to design and examine the effect of our new scheme on the performance of a 1 KB memory. But due to the limitations of the design software and the slow processing speed of a desktop PC, the integration of such large structure was not feasible ,so we had to scale down to an array of 64 cells.

5. ACKNOWLEDGEMENTS

With every dissertation there lies a scope for improvement and future work. Future work in this thesis might include a further scaling down of the technology node, which we could not accomplish due to unavailability of corresponding T-Spice model files in the initial stage of our research work. Improvement may also be devised for the proposed cell architecture so that its SNM may increase. Size of the memory can also be extended further.

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